CLAIMS:

1. An integrated circuit comprising a timing closure monitoring circuit for monitoring timing closure in a logic path on the integrated circuit, the timing closure monitoring circuit comprising:

- a signal generator for generating a predetermined reference signal;
- a duplicate logic path having characteristics matched with the logic path being monitored, and connected to receive the reference signal from the signal generator; and
- monitoring means arranged to receive an output signal from the duplicate logic path, and provide an output signal indicative of the status of the timing closure in the logic path being monitored.

2. An integrated circuit as claimed in claim 1, wherein the monitoring means is arranged to provide a timing closure violation signal when the output of the duplicate path is delayed by a predetermined amount.

3. An integrated circuit as claimed in claim 1 or 2, wherein the integrated circuit includes a clock signal for clocking the logic path being monitored, the clock signal also being used by the signal generator to generate the reference signal, and by the monitoring means for monitoring the status of the output of the duplicate logic path.

4. An integrated circuit as claimed in claim 3, wherein the reference signal produced by the signal generator is synchronized with the clock signal.

5. An integrated circuit as claimed in claim 4, wherein the reference signal is synchronized with the leading edge of the clock signal.

6. An integrated circuit as claims in any one of claims 3 to 5, wherein the reference signal produced by the signal generator is delayed with respect to the clock signal.

7. An integrated circuit as claimed in claim 6, wherein the reference signal is delayed with respect to the clock signal by an amount equal to (prop_delay)-(½ design_margin), where prop_delay is the propagation delay of a processing unit driving the logic path, and the design margin relates to the sensitivity of the circuit for detecting timing closure.

8. An integrated circuit as claimed in any one of the preceding claims, wherein the signal generator is configured to generate a reference signal having a pulse width that is predetermined according to a design margin.

9. An integrated circuit as claimed in claim 8, wherein the design margin determines the sensitivity of the timing closure monitoring circuit for detecting timing closure violation.

10. An integrated circuit as claimed in any one of the preceding claims, wherein the duplicate logic path is configured to match the delay and/or composition characteristics of the logic path being monitored.

11. An integrated circuit as claimed in claim 10, wherein the duplicate logic path includes one or more buffer stages for matching the characteristics of the logic path being monitored.

12. An integrated circuit as claimed in claim 11, wherein the buffer stages comprise the same number of switching gates as the logic path being monitored.

13. An integrated circuit as claimed in claim 2, wherein the timing closure violation signal is used to generate an interrupt signal.

14. An integrated circuit as claimed in claim 2, wherein the timing closure violation signal is supplied to a second timing closure monitoring circuit on the integrated circuit, the first and second timing closure monitoring circuits generating a serial interrupt signal.

15. An integrated circuit as claimed in any one of the preceding claims, wherein the logic path being monitored is a critical path in the integrated circuit.

16. An integrated circuit as claimed in any one of the preceding claims, having one or more further timing closure monitoring circuits, for monitoring timing closure in one or more further logic paths on the integrated circuit.

17. An integrated circuit as claimed in any one of the preceding claims, wherein the monitoring means comprises a latch.

18. An integrated circuit as claimed in any one of the preceding claims, wherein the output signal of the monitoring means is used to control the timing closure in the logic path being monitored.

19. A method of monitoring timing closure in a logic path on an integrated circuit, the method comprising the steps of:

- generating a predetermined reference signal;
- providing a duplicate logic path corresponding to the logic path being monitored;
- passing the reference signal through the duplicate logic path, and
- monitoring the output of the duplicate logic path, and using the output of the duplicate logic path to produce an output signal indicative of the status of the timing closure in the logic path being monitored.

20. A method as claimed in claim 19, wherein the output signal indicates timing closure violation when the output of the duplicate path is delayed by a predetermined amount.

21. A method as claimed in claim 19 or 20, wherein a clock signal provided for clocking the logic path is used to generate the reference signal, and for monitoring the output of the duplicate path.

22. A method as claimed in claim 21, wherein the reference signal is synchronized with the clock signal.

23. A method as claimed in claim 22, wherein the reference signal is delayed with respect to the clock signal.

24. A method as claimed in claim 23, wherein the reference signal is delayed with respect to the clock signal by an amount equal to (prop_delay)-(½ design_margin), where prop_delay is the propagation delay of a processing unit driving the logic path, and the design margin relates to the sensitivity of the circuit for detecting timing closure.

25. A method as claimed in any one of claims 19 to 24, wherein the pulse width of the reference signal is chosen according to a predetermined design margin.

26. A method as claimed in claim 25, wherein the design margin relates to the sensitivity of the timing closure monitoring circuit for detecting timing closure violation.

27. A method as claimed in any one of claims 19 to 26, wherein the duplicate logic path is configured to match the delay and/or composition characteristics of the logic path being monitored.

28. A method as claimed in any one of claims 19 to 27, wherein the logic path being monitored is a critical path in the integrated circuit.

29. A method as claimed in any one of claims 19 to 28, wherein the duplicate logic path is initially determined by:

- identifying a critical logic path in the integrated circuit;
- decomposing the critical path into one or more stages;
- constructing buffer stages corresponding to the stages identified in the decomposing step, the buffer stages being constructed to have the same characteristics as the stages of the critical path being monitored; and
- composing the duplicate path using the buffer stages constructed in the constructing step.